REMARKS

At the outset, the Examiner is thanked for the thorough review and consideration of the subject application. The Office Action of June 29, 2004 has been received and contents carefully reviewed.

By this Amendment, Applicant amends claim 82. Accordingly, claims 27-37 and 56-88 are currently pending in the present application. Reexamination and reconsideration of the application are respectfully requested.

In the Office Action, the Examiner objected to the drawings, stating that Figs. 11A and 13 should be designated by a legend such as "Prior Art." In response, Applicant has added a legend "Prior Art" to Fig. 11A. However, Applicant respectfully disagrees with the Examiner's objection to Fig. 13. Fig. 13 provides output waveform diagrams of one embodiment of the present invention disclosed in Fig. 12. See, for example, paragraph [0045] of the present application. Accordingly, Applicant respectfully requests the withdrawal of this objection.

In addition, the Examiner rejected claims 27-37 and 56-88 under 35 U.S.C. § 102(e) as being anticipated by Suzuki et al. (U.S. Patent No. 5,587,722), and rejected claims 35, 85 and 86 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al. in view of Applicant's Related Art (ARA). Applicant respectfully traverses these rejections.

The rejection of claims 27-37 and 56-88 under 35 U.S.C. § 102(e) as being anticipated by Suzuki et al. is respectfully traversed and reconsideration is requested. Claim 27 is allowable over the cited references in that claim 27 recites a combination of elements including, for example, "wherein the second voltage is near the data signal voltage..." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention.

Applicant respectfully submits that a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. See M.P.E.P. § 2131. As shown in Fig. 11B, in the present application, "the voltage level of the scanning signal SCS approaches to the voltage level of the data voltage signal DVS at the falling edge of the Scanning signal." See, for example, paragraph [0043] of the present application. However, Suzuki et al. fails to teach or suggest the aforementioned feature recited in

claim 27. Accordingly, Applicant respectfully submits that claim 27 and claims 28-37, which depend therefrom, are allowable over the cited references.

Claim 56 is allowable over the cited references in that claim 56 recites a combination of elements including, for example, "said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the second gate voltage, wherein the second gate voltage has a voltage level that turns off the switching transistor." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention.

Paragraph [0036] of the present application discloses, "[t]he TFT CMN included in the pixel 31 is turned on until a voltage of the scanning signal SCS from the gate line GL drops less than its threshold voltage. At this time, Although electric charges charged in a liquid crystal cell Clc are pumped into the gate line GL, sufficient electric charges are charged into the liquid crystal cell Clc by a data voltage signal DVS passing through the TFT CMN from a signal line SL. Accordingly, the voltage charged in the liquid crystal cell Clc does not drop. Then, since a voltage variation amount on the gate line GL is a threshold voltage of the TFT CMN in maximum when the voltage of the scanning signal SCS on the gate line GL drops down under the threshold voltage of the TFT CMN, a electric charge amount pumped from the liquid crystal cell Clc into the gate line GL becomes very small. As a result, a feed through voltage ΔVp can be suppressed sufficiently."

Thus, one of the principles of the present invention is to reduce the gate voltage level substantially equal to but higher than the threshold voltage of the pixel transistor (switching transistor) prior to turning off the pixel transistor. However, Suzuki et al. fails to teach or suggest the aforementioned feature recited in claim 56. Accordingly, Applicant respectfully submits that claim 56, and claims 57-61 and 65-70 which depend therefrom, are allowable over the cited references.

Claim 62 is allowable over the cited references in that claim 62 recites a combination of elements including, for example, "supplying the first gate voltage and the second gate voltage selectively via a switching device, to the gate lines, said switching device being controlled by the shift register, said first gate voltage reducing a voltage level substantially to a threshold voltage level but enough to maintain an on-state of the switching transistor prior to transitioning to the

second gate voltage." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 62 and claims 63-64 which depend therefrom, are allowable over the cited references.

Claim 71 is allowable over the cited references in that claim 71 recites a combination of elements including, for example, "a gate driver connected to the plurality of scanning signal lines, said gate driver receiving first and second control voltages and a scanning clock signal and, in response to the scanning clock signal, successively outputting the first control voltage to the scanning signal lines to drive the scanning signal lines, wherein the switching device of each pixel responds to the first control voltage to connect the first electrode with the pixel electrode, and responds to the second control voltage to disconnect the first electrode from the pixel electrode, wherein a voltage level of the first control voltage received by the gate driver changes during a period of the scanning clock signal prior to the driver selecting a successive scanning line, and wherein the voltage level of the first control voltage turns on the switching device and the voltage level of the first control voltage is reduced substantially to a threshold voltage level but enough to maintain an on-state of the switching device during the period of the scanning clock signal prior to the driver selecting the successive scanning line." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 71, and claims 72-75 which depend therefrom, are allowable over the cited references.

Claim 76 is allowable over the cited references in that claim 76 recites a combination of elements including, for example, "sequentially applying a first voltage to each of the plurality of scanning lines, wherein the first voltage electrically connects the plurality of contact electrodes to the plurality of pixel electrodes; and sequentially applying a second voltage to each of the plurality of scanning lines, wherein the second voltage electrically disconnects the plurality of contact electrodes from the plurality of pixel electrodes, wherein the second voltage is sequentially applied to each of the plurality of scanning lines after the application of the first voltage to each of the plurality of scanning lines but prior to the sequential application of the first voltage to another one of the plurality of scanning lines." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention. Accordingly, Applicant respectfully submits that claim 76, and claims 77-81 which depend therefrom, are allowable over the cited references.

Claim 82 is allowable over the cited references in that claim 82 recites a combination of elements including, for example, "a high level gate voltage generator and a low level gate voltage generator electrically connected to the gate driver and outputting the first and second voltage levels to the gate driver, respectively, the high level gate voltage generator including a means for modulating the first voltage level of the gate signal..." None of the cited references, singly or in combination, teaches or suggests at least this feature of the claimed invention.

In Fig. 3 of Suzuki et al., two voltage sources VVDD and VCKX are connected to the shift register 3 which is part of the vertical scanning circuit (gate driver). As discussed in the present application, the circuit disclosed in Suzuki et al. has the following disadvantages: "shift register must be driven at a high voltage because the power supply voltage VVDD is equal to a high-level gate voltage to be applied to gate lines on the liquid crystal display panel. In the other word, inverters included in the shift register operate at about 25 V of the driving voltage. Due this end, the active matrix liquid crystal display device disclosed in U.S. Pat. No. 5,587,722 consumes a large amount of power." See paragraph [0010] of the present application. Furthermore, in contrast to the circuit disclosed in Suzuki et al., the high level gate voltage generator in the present application, which is a separate element different from the gate driver, has "a means for modulating the first voltage level of the gate signal." Accordingly, Applicant respectfully submits that claim 82 and claims 83-88 which depend therefrom, are allowable over the cited references.

The rejection of claims 35, 85 and 86 under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al. in view of ARA is respectfully traversed and reconsideration is requested. Applicant respectfully submits that since ARA fails to cure the deficiencies of Suzuki et al. as discussed above, claims 35, 85 and 86 are allowable over the cited references.

Applicant believes the foregoing amendments place the application in condition for allowance and early, favorable action is respectfully solicited. Should the Examiner deem that a telephone conference would further the prosecution of this application, the Examiner is invited to call the undersigned attorney at the telephone number (202) 496 – 7500. All correspondence should continue to be sent to the below-listed address.

If these papers are not considered timely filed by the Patent and Trademark Office, then a petition is hereby made under 37 C.F.R. §1.136, and any additional fees required under 37

C.F.R. §1.136 for any necessary extension of time, or any other fees required to complete the filing of this response, may be charged to Deposit Account No. 50-0911. Please credit any overpayment to deposit Account No. 50-0911.

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Respectfully submitted,

By

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Attachments

ANNOTATED SHEET SHOWING CHANGES

ANNOTATED MARKED-UP
DRAWINGS

FIG.11A
PRIOR ART

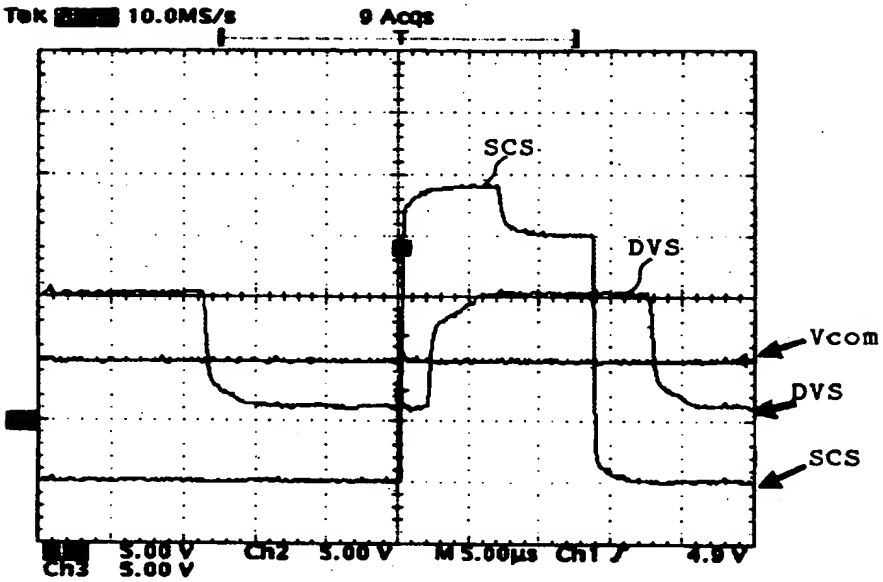

FIG.11B